UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,295	06/24/2003	Yoshiyuki Arai	10873.1243US01	9034

23552 7590 11/18/2004

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,295	ARAI ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of group I in the reply filed on 09/01/04 is acknowledged. The traversal is on the ground(s) that the restriction is not proper. This is not found persuasive because group II (claims 13-19) and group I (claims 1-12) are related as process of making and product made, respectively. Additionally, the device of group I (claims 1-12) invention could be made by as a materially different process. For example, by manual applications, using brush coating to expose a part of side surfaces of the semiconductor chip to the outside of the encapsulation resin layer, instead of injecting or transferring the encapsulation resin into the space of mold to exposed the part of side surfaces of the semiconductor chip to the outside of the encapsulation resin layer.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 5, 6 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,583,502 to Lee et al.

Regarding claim 1, Lee et al. (figures 1A-2) teach a semiconductor device comprising:

a substrate (180);

a plurality of semiconductor chips (130, 130') mounted on the substrate (180) by stacking one on top of another; and

an encapsulation resin layer (177),

wherein, among the plurality of semiconductor chips, a first semiconductor chip (130') as an uppermost semiconductor chip (an upper chip [130']) is mounted with a surface thereof on which a circuit (a lower active surface of chip [130']) is formed facing the substrate (180), and wherein the encapsulation resin layer (177) is formed so that at least a surface (an upper surface of the chip [130']) of the first semiconductor chip (130') opposite to the surface (a lower surface of the chip [130'] on which the circuit is formed and a part of side surfaces (a side conner portion of the chip [130']) of the first semiconductor chip (130') are exposed to the outside of the encapsulation resin layer (177).

Regarding claim 3, Lee et al. teach the first semiconductor chip (130') and a second semiconductor chip (130) provided immediately below the first semiconductor chip (130') is electrically connected to each other via bumps (the first chip [130'] is connected to the second chip [130] by bumps [150] through wires [140, 140']).

Regarding claim 5, Lee et al. teach a lowermost semiconductor chip (chip [130]) is electrically connected to the substrate (120) via a wire (140).

Regarding claim 6, Lee et al. teach the bumps (150) form a space (a space is between the chip [130'] and chip [130]) between the first semiconductor chip (130') and the second

semiconductor chip (130), and the space (a space is between two chips [130', 130]) is filled with the encapsulation resin (177 or 170) of the encapsulation resin layer.

Regarding claim 9, Lee et al. teach on a second semiconductor chip (right chip [230']) provided immediately below the first semiconductor chip (chip [230] is formed below the right chip [230']), a third semiconductor chip (left chip [230']) is mounted along with the first semiconductor chip (right chip [230']) (figure 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,583,502 to Lee et al. in view of US Patent No. 6,340,846 to LoBianco et al.

Regarding claim 2, Lee et al. differ from the claimed invention by not showing a lowermost semiconductor chip is bonded to the substrate with an adhesive. However, LoBianco et al. (figures 1-8) teach a lowermost semiconductor chip (a lower chip [14]) is bonded to the substrate (12) with an adhesive (13). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of LoBianco et al. into the device taught by Lee et al. because it is desirable securely to hold the chip in place.

Regarding claim 4, Lee et al. differ from the claimed invention by not showing a portion of the first semiconductor chip is bonded to a portion of the second semiconductor chip with an

adhesive. However, LoBianco et al. (figures 1-8) teach a portion of the first semiconductor chip (16) is bonded to a portion of the second semiconductor chip (14) with an adhesive (42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of LoBianco et al. into the device taught by Lee et al. because it is securely to hold the chips in place.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,583,502 to Lee et al. in view of US Patent No. 5,900,669 to Knapp et al.

Regarding claim 7, Lee et al. differ from the claimed invention by not showing the substrate is a lead fame. However, Knapp et al. teach the substrate is a lead frame (column 1, lines 9-11). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Knapp et al. into the device taught by Lee et al. because it provides input/output terminals connection between the chip and the substrate. Additionally, the leadframe substrate is flexible and capable of withstanding the clamping pressures of the mold tool.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Knapp et al., and further in view of US Patent No. 6,433,277 to Glenn.

Regarding claim 8, the disclosures of Lee et al. and Knapp et al. are discussed as applied to claim 7 above.

The combined device differs from the claimed invention by not showing a lowermost semiconductor chip is bonded to one surface of a die pad portion of the leadfame, and wherein

the encapsulation resin layer is formed so the other surface of the die pad portion is exposed to the outside of the encapsulation resin layer. However, Glenn (figure 8) teaches a semiconductor chip (56) is bonded to one surface of a die pad portion (24) of the leadframe (53), and wherein the encapsulation resin layer (40) is formed so the other surface of the die pad portion (a lower surface of the die pad [24]) is exposed to the outside of the encapsulation resin layer (40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Glenn into the device taught by Lee et al. and Knapp et al. because it provides an interconnection between the chip and the external terminal.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of US Patent No. 5,701,233 to Carson et al.

Regarding claim 10, Lee et al. differ from the claimed invention by not showing both the first semiconductor chip and the third semiconductor chip are electrically connected to the second semiconductor chip via bumps. However, Carson et al. (figure3) teach the first and third semiconductor chip (left and right chip) are electrically connected to the second chip (lower chip). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Carson et al. into the device taught by Lee et al. because it increase the operation of the device. The combined device shows both the first semiconductor chip and the third semiconductor chip are electrically connected to the second semiconductor chip via bumps.

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of US Patent No. 6,069,023 to Bernier et al.

Regarding claim 11, Lee et al. differ from the claimed invention by not showing a heat dissipator is provided on the surface of the first semiconductor chip exposed to the outside of the encapsulation resin layer. However, Bernier et al. (figure 4) teach a heat dissipator (heat sink [246]), which is provided on the surface of the semiconductor chip (248) exposed to the outside of the encapsulation resin layer. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bernier et al. into the device taught by Lee et al. because it dissipates heat from the chip. The combined device shows a heat dissipator is provided on the surface of the first semiconductor chip exposed to the outside of the encapsulation resin layer.

Regarding claim 12, the combined device shows the heat dissipator is a metal heat sink (Bernier et al.; heat sink [246]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
November 12, 2004

Sara Crane
Primary Examiner